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ACORN 32K D. RAM

TECHNICAL MANUAL
100, 010/3

SG/CDP/300382

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INTRODUCTION

The Acorn 32K Dynamic R.A.M. Board provides either 16K or 32K of user R.A.M. space and connects to the standard Acorn bus via a 64 way euro-connector, the Board is fully buffered to ensure a low loading on the bus. The 32K Dynamic R.A.M. Board may be freely mixed with other static R.A.M. boards.

The 16K and 32K cards operate from a single (positive) 5 volt supply and the current consumption is not more than 300 milli-amps in its maximum configuration.

The Dynamic R.A.M. Card needs a number of timing signals for operation, which may be obtained in one of two ways:

1. When used in conjunction with the Acorn 6502 CPU card or Atom, the signals are generated on the R.A.M. board from (phase) 2.

2. When used with the Acorn 6502A CPU card all the signals are generated on the CPU card.

For more details on the above see page 7

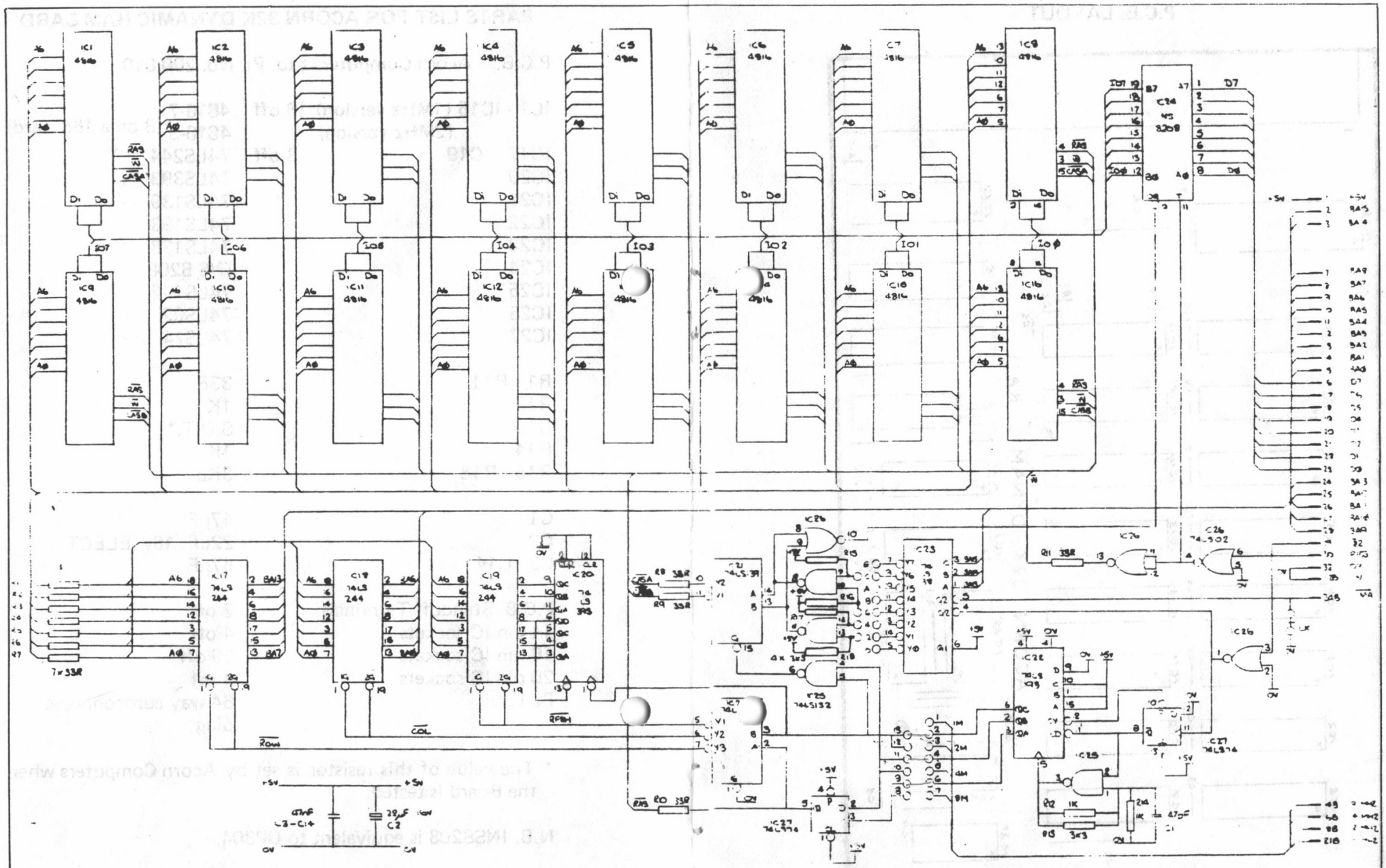
PARTS LIST FOR ACORN 32K DYNAMIC RAM CARD

P.C.B. Acorn Computers Ltd. Pt. No. 200.010

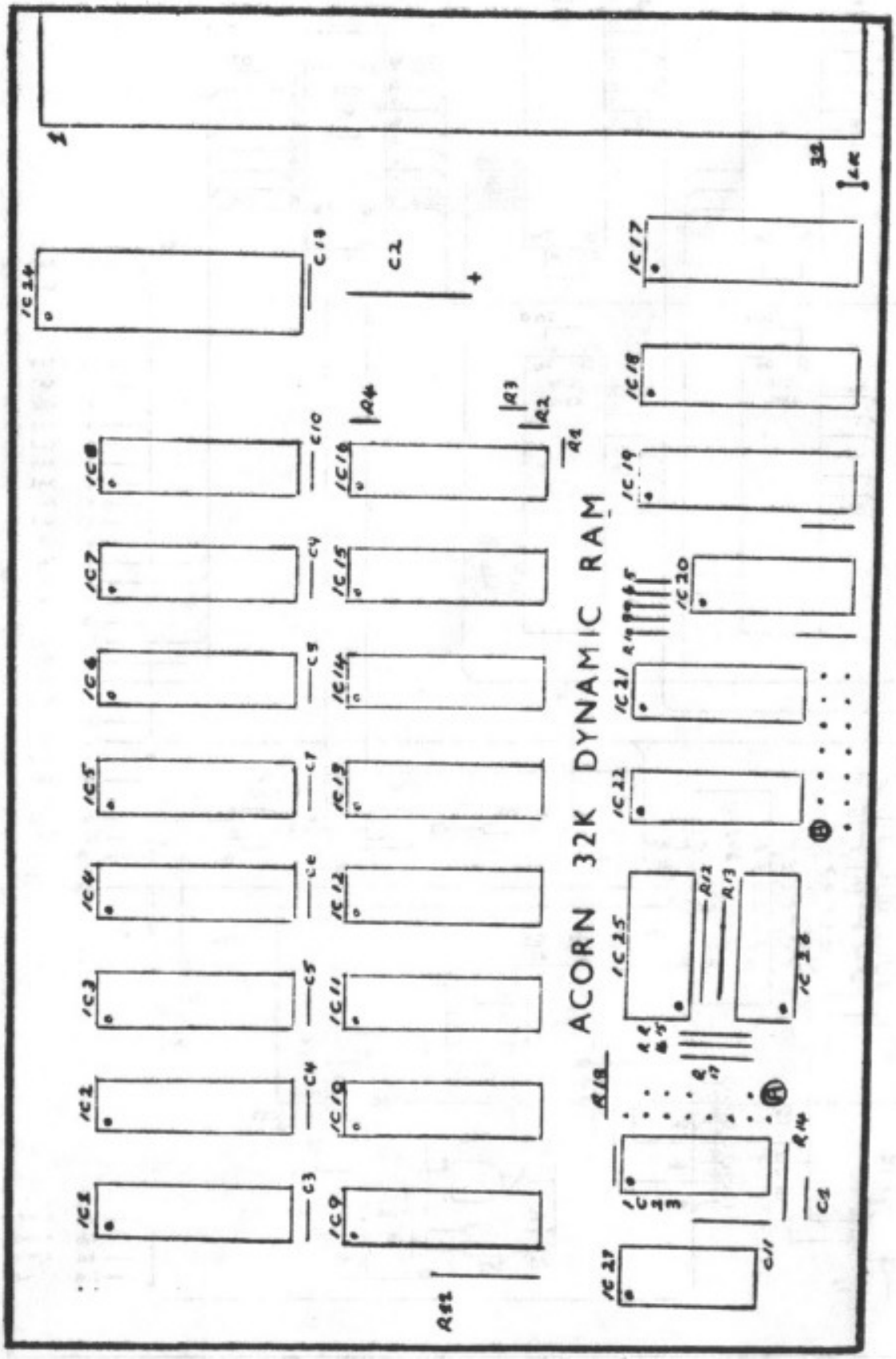
IC1 - IC16 (1MHz version)	16 off	4816-7
(2MHz version)		4816-3 (8 on a 16K card)
IC17 - IC19	3 off	74LS244
IC20		74LS393
IC21		74LS139
IC22		74LS193
IC23		74LS138
IC24		INS 8208
IC25		74LS132
IC26		74LS02
IC27		74LS74
R1 - R11		33R
R12		1K
R13		S.O.T.*
R14		1K
R15 - R18		3K3
C1		47pF
C2		22uF 16v ELECT
C3 - C14		47nF
P.C.B. Standoff Terminals		2 off
14 pin IC sockets		4 off
16 pin IC sockets		19 off
20 pin IC sockets		4 off
PL1		64 way euroconnector plug

* The value of this resistor is set by Acorn Computers when the Board is tested.

N.B. INS8208 is equivalent to DP304.


IC1 4816
IC2 4816
IC3 4816
IC4 4816
IC5 4816
IC6 4816
IC7 4816
IC8 4816
IC9 4816
IC10 4816
IC11 4816
IC12 4816
IC16 4816
IC24 MS 8208
IC17 74LS 244
IC18 74LS 244
IC19 74LS 244
IC20 74LS 393
IC21 74LS 139
IC22 74LS 08
IC23 74LS 153
IC25 74LS 32
IC26 74LS 02
IC27 74LS 74
IC28 74LS 00
7×33R
4×3K3
47nF C3-C14
22μF C2
ROW
COL
RFSH
RAS
CAS
ACORN COMPUTERS LTD

P.C.B. LAYOUT



ADDRESS SELECTION

Two sets of links can be found on the Dynamic R.A.M. Board. The set furthest from the edge connector (marked 'A' on the layout, page 5) is associated with the address selection.

As you will note, there are two columns of pins. The left-hand column determines the start address of the 8K Blocks, ie 0000, 2000, 4000, 6000 . . . E000 (hexadecimal). The righthand column of 4 pins are the control lines for the four 8K Blocks present when the Board is fully populated, Pins 1 and 2 (uppermost pair) control the upper row of R.A.M. Chips (IC's 9-16). When the Board is populated as a 16K store either the complete upper row or complete lower row may be used. **R.A.M. Chips cannot be distributed between the rows.**

To enable the Board to be mappable on 8K boundaries a certain amount of address decoding redundancy is inevitable, thus the following mapping restrictions must be observed:

> The block of Memory remaining unaddressed between the addresses that pins 1 and 2 control (or pins 3 and 4), must NOT be 8K, 24K, or 40K, (a difference of 2000, 6000, or A000 hex), and therefore will be 0K, 16K, 32K, 04 48K (a difference of 0000, 4000, 8000, or C000 hex).

The usual configuration of a 32K Board in an Acorn system is blocks of memory at 2000, 4000, 6000 and C000 (hex). A further 16K Board can then be used to deal with 8000, A000 (hex).

CLOCK SELECTION

Using the 32K Dynamic R.A.M. Board with Acorn products results in the following clock arrangements becoming necessary.

You will note that there are 13 linking positions in the middle of the bottom of the Board (marked 'B' on layout). These enable the card to be configured for different environments.

For the Atom and Acorn 6502 CPU card (used in current systems 1 - 4). In these environments the memory card's clock signals must be derived from Ø (phase) 2 on the CPU. To do this link Pin 2 to Pin 13; Pin 4 to Pin 11; Pin 6 to Pin 9.

For the Acorn 6502A CPU card (to be used in future equipment). All the necessary clock signals for the 32K memory card are generated on this CPU card. The links necessary for this environment are:

CPU running at 1MHz --
Pin 1 to Pin 13; Pin 3 to Pin 11; Pin 5 to Pin 9

CPU running at 2MHz —
Pin 3 to Pin 12; Pin 5 to Pin 10; Pin 7 to Pin 8

V.M.A.

A link is provided to allow Valid Memory Addressing if such a signal is present on the bus (not applicable on a standard Acorn system). To utilize the "paging" facility offered by this, the tracking **between** the two plated through holes should be cut. NOTE: If this is done without a V.M.A. signal being present it will disable the card from the system.