

## DM54S570/DM74S570 open-collector 2048-bit PROM DM54S571/DM74S571 TRI-STATE® 2048-bit PROM

### general description

These Schottky memories are organized in the popular 512 words by 4 bits configuration. A memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word.

If the enable input is raised to a high level, it causes all 4 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as ROM's as well as PROM's.

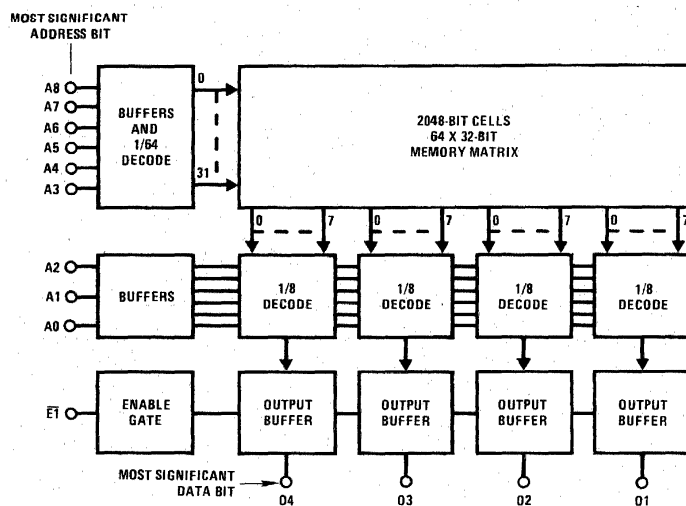
PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

### features

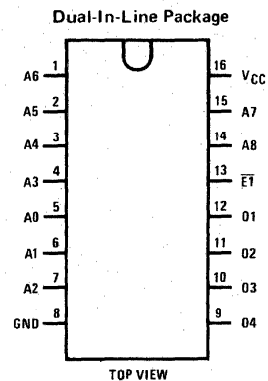
- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed  
Address access—55 ns max  
Enable access—30 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- ROM mates are DM74S270 and DM74S370

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S570		X	X		N, J
DM74S571		X		X	N, J
DM54S570	X		X		J
DM54S571	X			X	J

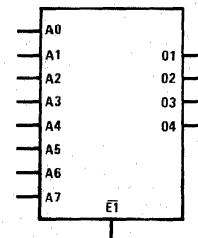
### block diagram



### connection diagram



### logic symbol



**absolute maximum ratings** (Note 1)

Supply Voltage (Note 2)	-0.5V to +7V
Input Voltage (Note 2)	-1.2V to +5.5V
Output Voltage (Note 2)	-0.5V to +5.5V
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

**operating conditions**

	MIN	MAX	UNITS
Supply Voltage (V <sub>CC</sub> )			
DM54S570, DM54S571	4.5	5.5	V
DM74S570, DM74S571	4.75	5.25	V
Ambient Temperature (T <sub>A</sub> )			
DM54S570, DM54S571	-55	+125	°C
DM74S570, DM74S571	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

**dc electrical characteristics** (Note 3)

PARAMETER	CONDITIONS	DM54S570, 54S571			DM74S570, 74S571			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
I <sub>IL</sub>	Input Load Current, All Inputs	V <sub>CC</sub> = Max, V <sub>IN</sub> = 0.45V		-80	-250		-80	-250	μA
I <sub>IH</sub>	Input Leakage Current, All Inputs	V <sub>CC</sub> = Max, V <sub>IN</sub> = 2.7V			25			25	μA
I <sub>I</sub>	Input Leakage Current, All Inputs	V <sub>CC</sub> = Max, V <sub>IN</sub> = 5.5V			1.0			1.0	mA
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = 16 mA		0.35	0.5		0.35	0.5	V
V <sub>IL</sub>	Low Level Input Voltage				0.80			0.80	V
V <sub>IH</sub>	High Level Input Voltage			2.0			2.0		V
I <sub>CEX</sub>	Output Leakage Current (Open-Collector Only) (Note 5)	V <sub>CC</sub> = Max, V <sub>CEX</sub> = 2.4V			50			50	μA
		V <sub>CC</sub> = Max, V <sub>CEX</sub> = 5.5V			100			100	μA
V <sub>C</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>IN</sub> = -18 mA		-0.8	-1.2		-0.8	-1.2	V
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 5V, V <sub>IN</sub> = 2V, T <sub>A</sub> = 25°C, 1 MHz		4.0			4.0		pF
C <sub>O</sub>	Output Capacitance	V <sub>CC</sub> = 5V, V <sub>O</sub> = 2V, T <sub>A</sub> = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I <sub>CC</sub>	Power Supply Current	V <sub>CC</sub> = Max, All Inputs Grounded, All Outputs Open		90	130		90	130	mA

**TRI-STATE PARAMETERS**

I <sub>SC</sub>	Output Short Circuit Current (Note 5)	V <sub>O</sub> = 0V, V <sub>CC</sub> = Max, (Note 4)	-30	-60	-100	-30	-60	-100	mA
I <sub>HZ</sub>	Output Leakage (TRI-STATE)	V <sub>CC</sub> = Max, V <sub>O</sub> = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V <sub>OH</sub>	Output Voltage High, (Note 5)	I <sub>OH</sub> = -2 mA	2.4	3.2					V
		I <sub>OH</sub> = -6.5 mA				2.4	3.2		V

**ac electrical characteristics** (With standard load)

PARAMETER	CONDITIONS	DM54S570, 54S571			DM74S570, 74S571			UNITS	
		5V ±10%; -55°C to +125°C							
		MIN	TYP	MAX	MIN	TYP	MAX		
t <sub>AA</sub>	Address Access Time	(Figure 1)		40	65		40	55	ns
t <sub>EA</sub>	Enable Access Time	(Figure 2)		20	35		20	30	ns
t <sub>ER</sub>	Enable Recovery Time	(Figure 2)		20	35		20	30	ns

**Note 1:** Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

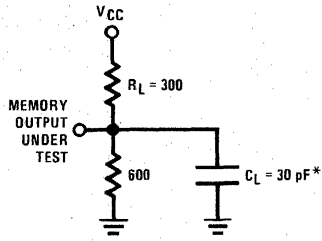
**Note 2:** These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

**Note 3:** These limits apply over the entire operating range unless stated otherwise. All typical values are for V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C.

**Note 4:** During I<sub>SC</sub> measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

**Note 5:** To measure V<sub>OH</sub>, I<sub>CEX</sub> or I<sub>SC</sub> on an unprogrammed part, apply 10.5V to both A8 and A2 (pin 14 and pin 7).

**standard test load**



\*CL includes probe and jig capacitance.

- Input waveforms are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, ZOUT = 50Ω, tr ≤ 2.5 ns and tf ≤ 2.5 ns (between 1.0V and 2.0V).
- tAA is measured with both enable inputs at a steady low level.
- tEA and tER are measured from the 1.5V on inputs and outputs with all address inputs at a steady level and with the unused enable input at a steady low level.

**switching time waveforms**

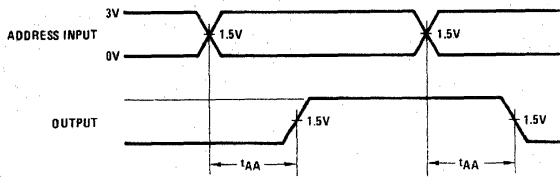


FIGURE 1. Address Access Time

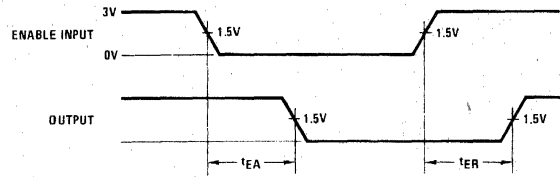
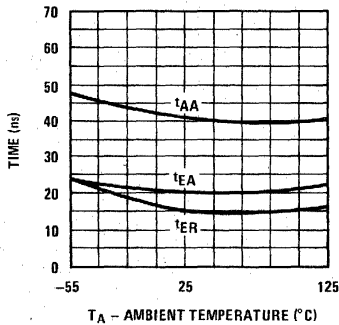


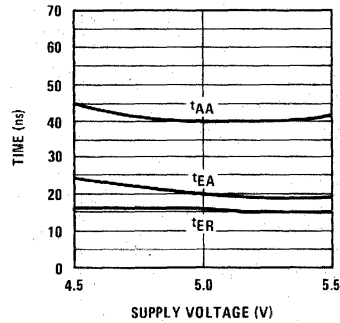
FIGURE 2. Enable Access Time and Recovery Time

**typical performance characteristics**

Typical Switching Characteristics as a Function of Temperature (VCC = 5V, Standard Load)

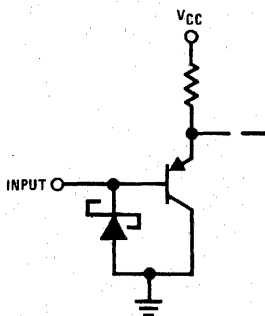


Typical Switching Characteristics as a Function of VCC (TA = 25°C, Standard Load)

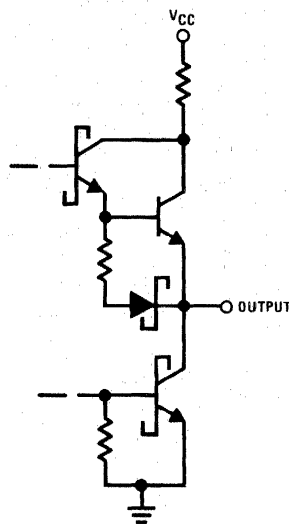


**equivalent circuits**

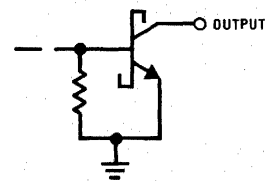
Equivalent of Each Input



Typical TRI-STATE Output

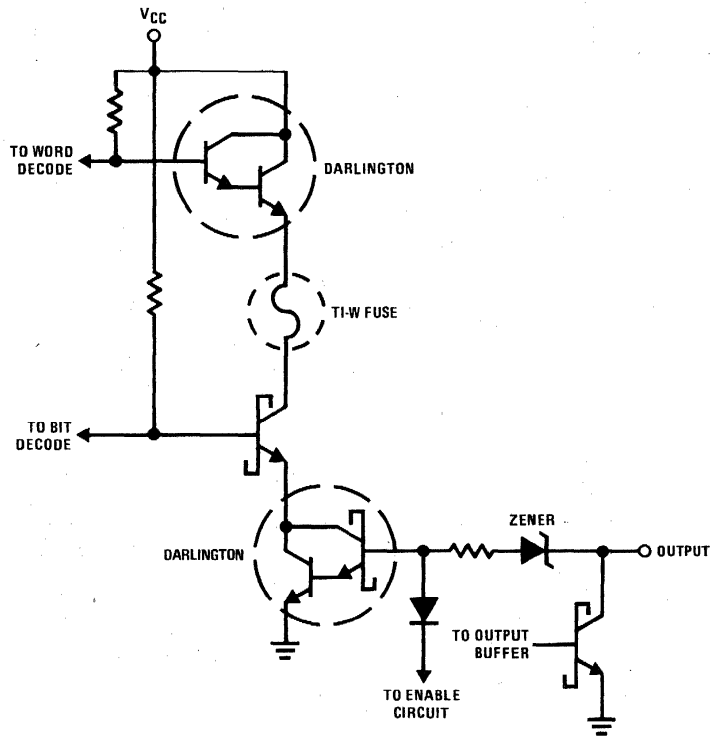


Typical Open-Collector Output



## equivalent circuits (Continued)

Programming Equivalent Circuit for One Memory Output  
(Applies to All NSC Generic Schottky PROMs)



## programming procedure

These parts are shipped from the factory with all fuses intact. As a result, the outputs will be low (logical "0") for all addresses. In order to generate a high level on the outputs, the part must be programmed. Information on available programming equipment may be obtained from National. However, if it is desired to build your own programmer, the following conditions must be observed.

1. Programming should be attempted only at temperatures between 15°C and 30°C.
2. Addresses and chip enable pins must be driven from normal TTL logic levels during both programming and verification.
3. Programming will occur at a selected address when  $V_{CC}$  is held at 10.5V, the appropriate output is held at 10.5V and the chip is subsequently enabled. To achieve these conditions in the appropriate sequence, the following procedure must be followed:
  - a) Select the desired word by applying a high or low level to the appropriate address inputs. Disable the chip by applying a high level to the enable input.
  - b) Increase  $V_{CC}$  to 10.5V  $\pm 0.5V$  with the rate of increase being between 1.0 and 10.0 V/ $\mu s$ . Since  $V_{CC}$  supplies the current to program the fuse as well as the  $I_{CC}$  of the device at programming voltage, it must be capable of supplying 400 mA at 11.0V.
  - c) Select the output where a high level is desired by raising that output voltage to 10.5V  $\pm 0.5V$ . Limit the rate of increase to a value between 1.0 and 10.0 V/ $\mu s$ . This voltage change may occur simultaneously with the increase in  $V_{CC}$  but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or tied to a high impedance source of at least 20 k $\Omega$ . (Remember that the outputs of the device are still disabled at this time because the chip enable is high.)

**programming procedure** (Continued)

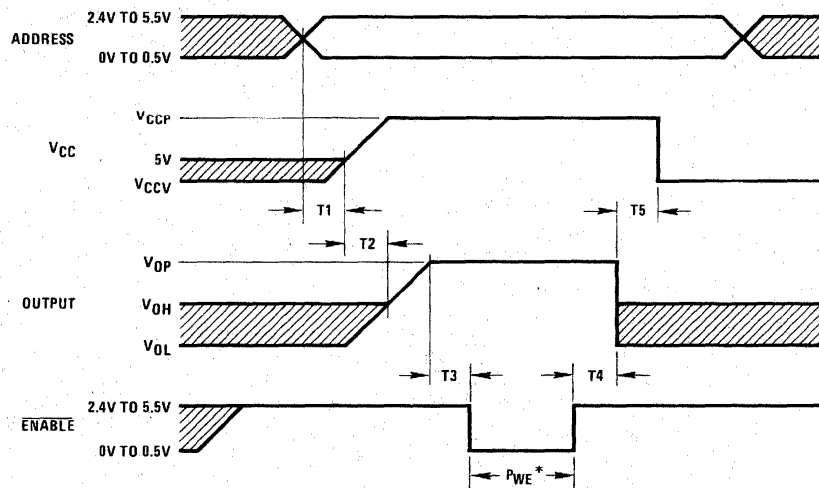
- d) Enable the device by taking the chip enable to a low level. This is done with a pulse of 10  $\mu$ s. The 10  $\mu$ s duration refers to the time that the circuit is enabled. Normal input levels are used and rise and fall times are not critical.
- e) Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing  $V_{CC}$  to 4.0V  $\pm$ 0.2V. Verification at a  $V_{CC}$  level of 4.0V will guarantee proper output states over the  $V_{CC}$  and temperature range of the programmed part. The chip must be enabled to sense the state of the outputs. During verification, the loading of the output must be within specified  $I_{OL}$  and  $I_{OH}$  limits. Steps b, c and d must be repeated 10 times or until verification that the bit has programmed.
- f) Following verification, apply five additional programming pulses to the bit being programmed. The programming procedure is now complete for the selected bit.
- g) Repeat steps a through f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of  $V_{CC}$  at programming voltage must be limited to a maximum of 25%. This is necessary to minimize chip junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.

Note: Since only an enabled chip is programmed, it is possible to program these parts at the board level if all programming parameters are complied with.

**programming parameters** Do not test or you may program the device.

PARAMETERS		CONDITIONS	MIN	RECOMMENDED VALUE	MAX	UNITS
$V_{CCP}$	Required $V_{CC}$ for Programming		10.0	10.5	11.0	V
$I_{CCP}$	$I_{CC}$ During Programming	$V_{CC} = 11V$			400	mA
$V_{OP}$	Required Output Voltage for Programming		10.0	10.5	11.0	V
$I_{OP}$	Output Current while Programming	$V_{OUT} = 11V$			20	mA
$t_{RR}$	Rate of Voltage Change of $V_{CC}$ or Output		1.0		10.0	V/ $\mu$ s
$P_{WE}$	Programming Pulse Width (Enabled)		9	10	11	$\mu$ s
$V_{CCV}$	Required $V_{CC}$ for Verification		3.8	4.0	4.2	V
$M_{DC}$	Maximum Duty Cycle for $V_{CC}$ at $V_{CCP}$			25	25	%

**programming waveforms**



- T1 = 100 ns min
- T2 = 5  $\mu$ s min (T2 may be  $\geq$  0 if  $V_{CCP}$  rises at the same rate or faster than  $V_{OP}$ )
- T3 = 100 ns min
- T4 = 100 ns min
- T5 = 100 ns min

\* $P_{WE}$  is repeated for 5 additional pulses after verification of  $V_{OH}$  indicates a bit has programmed